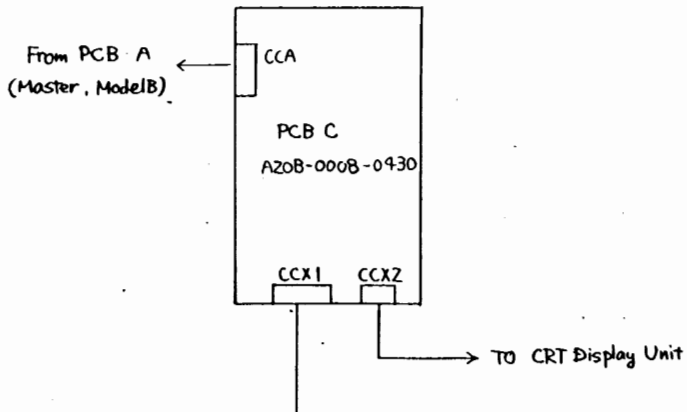


AWI-319434 / 18



C14 MR-20RMH

14	CH4	8	SG	1	PR
15	CH5	9	SD	2	TE
16	CH6	10	OV	3	ERR
17	CH7	11	CH1	4	TTY3
18	CH8	12	CH2	5	+6V
19	CH9	13	CH3	6	TTY2
20	PI			7	TTY1

ASR33, FACIT4010 Interface

C15 DBM-25S

14		1	SG
15		2	SD
16		3	RD
17		4	RS
18		5	CS
19		6	DR
20	ER	7	OV
21		8	CD
22		9	
23		10	
24		11	
25	+24V	12	
		13	

RS-232C Interface

Cable

CCA MR-50MA

32	*A02X	1	*A01X
33	*A04X	2	*A03X
34	*A07X	3	*A05X
35	*A10X	4	*A08X
37	*A13X	5	*A11X
38	*A16X	6	*A14X
39	BAUD	7	OV
40	CLKO	8	OV
41	-15V	9	OV
42	OV	10	+5V
43	+24V	11	+5V
44	*EXRBY	12	+5V
45	D02X	13	D01X
46	D05X	14	D03X
47		15	D06X
48		16	
49		17	
50		18	

CCX1 MR-50MA

23		1	TTY1
24	RS	2	TTY2
25	CS	3	TTY3
26	DR	4	OV
27	OV	5	
28	CD	6	
29	OV	7	PR
30	SD	8	TE
31	RD	9	ERR
32	OV	10	+6V
33	ER	11	CH1
34		12	CH2
35		13	CH3
36	SD	14	CH4
37	OV	15	CH5
38	CH9	16	CH6
39	PI	17	CH7
40	SG	18	CH8

CCX2 MR-20RMA

14	CLKINH	8	OV	1	VIDEO
15	EXCLKI	9	OV	2	HSYNC
16	DTCZ	10	OV	3	VSNC
17	EXCLKO	11	OV	4	
18		12	OV	5	
19		13	OV	6	
20	SG			7	

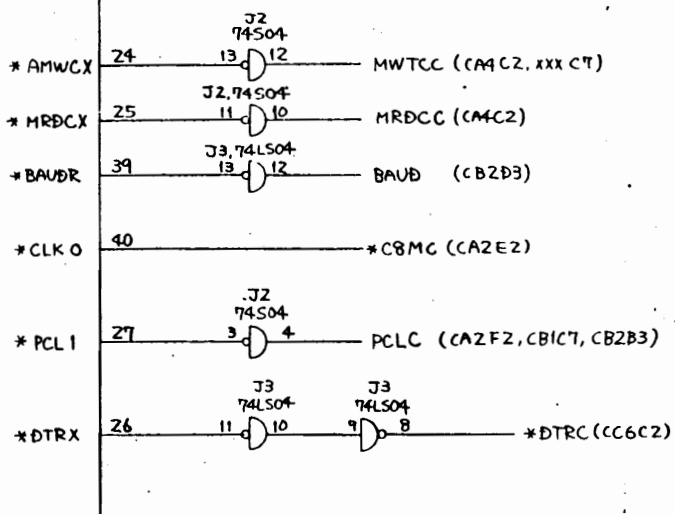
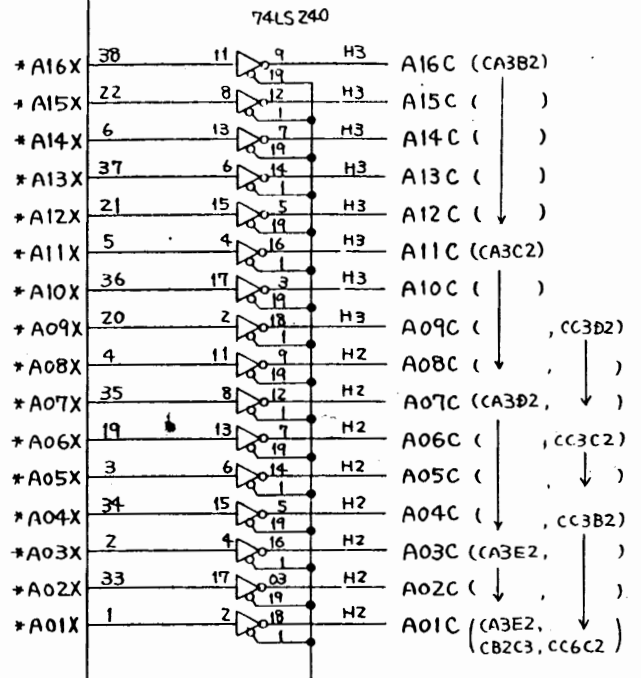
② Note: For Edition 01A, refer to the circuit before revised to 02 and Page 015A.01B
 注) 01A版以下は、02版改修前の回路図(01A、01B、01C、01D)を参照してください。(Appendix 41 In 02)

14-PIN IC

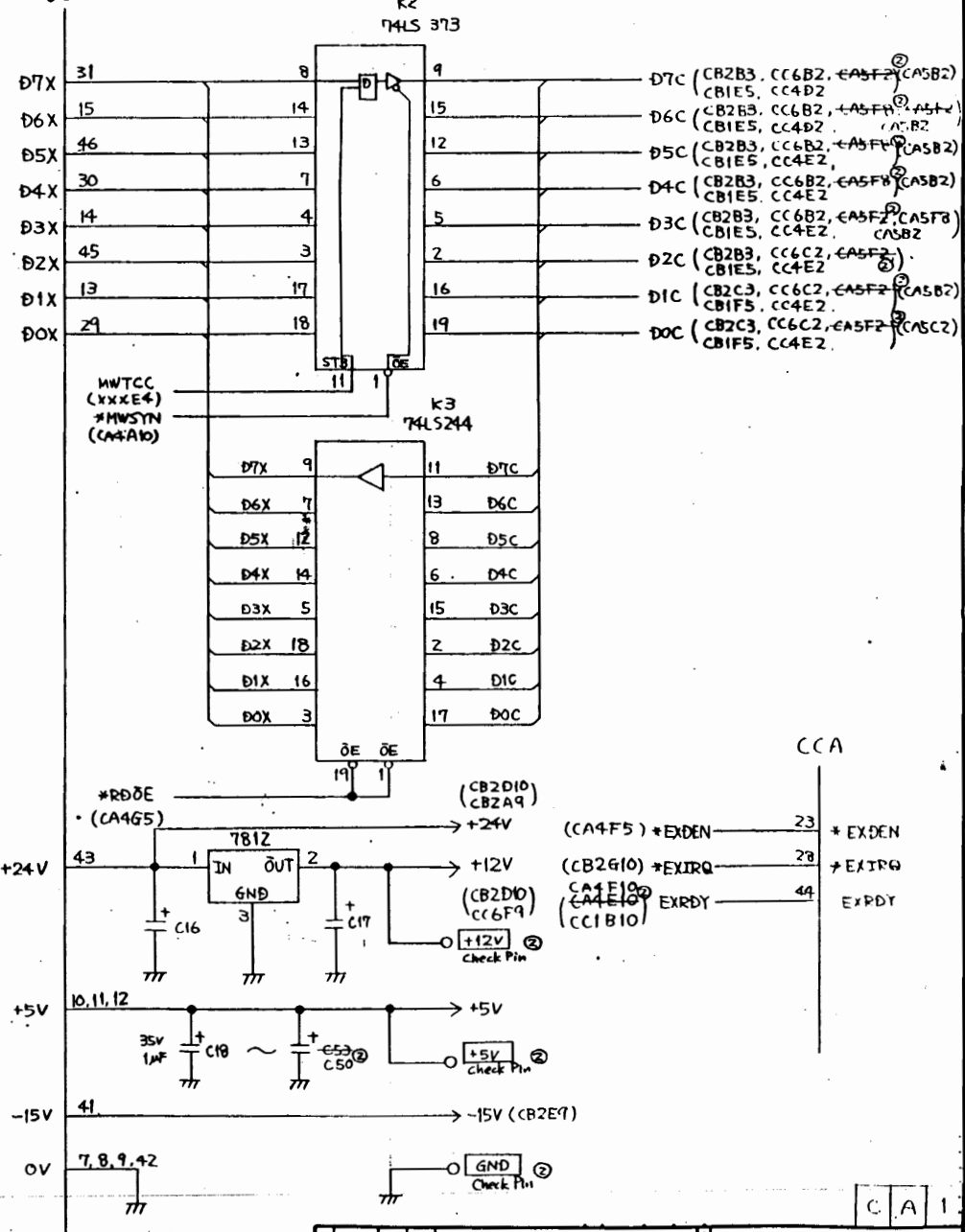
C 0 1
 CRTC/PUNCHER
 AZOC-0008-0430/01

AWT 319435 20

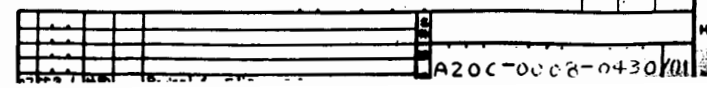
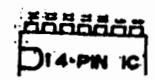
CCA



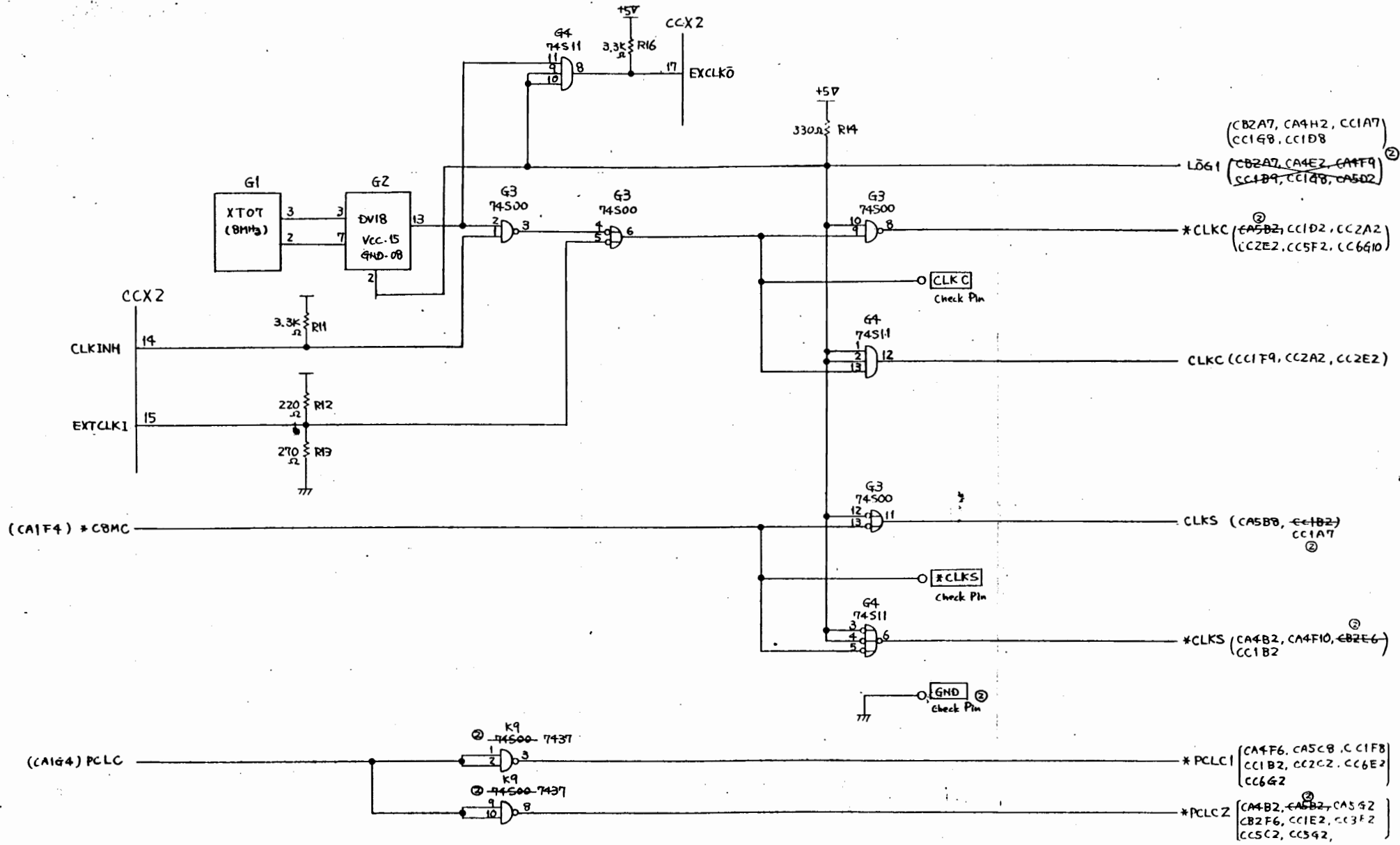
CCA



Interface for Master PCB



AW1 319436



(CB2A7, CA4H2, CCI1A7)
CCI1A8, CCI1B8

LOG1 (CB2A7, CA4E2, CA1F9)
CCI1B9, CCI1A8, CA5D2

*CLKC (CA5B2, CCI1D2, CC2A2)
CC2E2, CC5F2, CC6G10

CLKC (CC1F9, CC2A2, CC2E2)

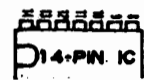
CLKS (CA5B8, CA1B2)
CCI1A7

*CLKS (CA4B2, CA4F10, CA2E6)
CCI1B2

*PCLC1 (CA4F6, CA5C8, CCI1F8)
CCI1B2, CC2C2, CC6E2
CC6G2

*PCLC2 (CA4B2, CA5B2, CA5G2)
CB2F6, CCI1E2, CC3F2
CC5C2, CC5G2

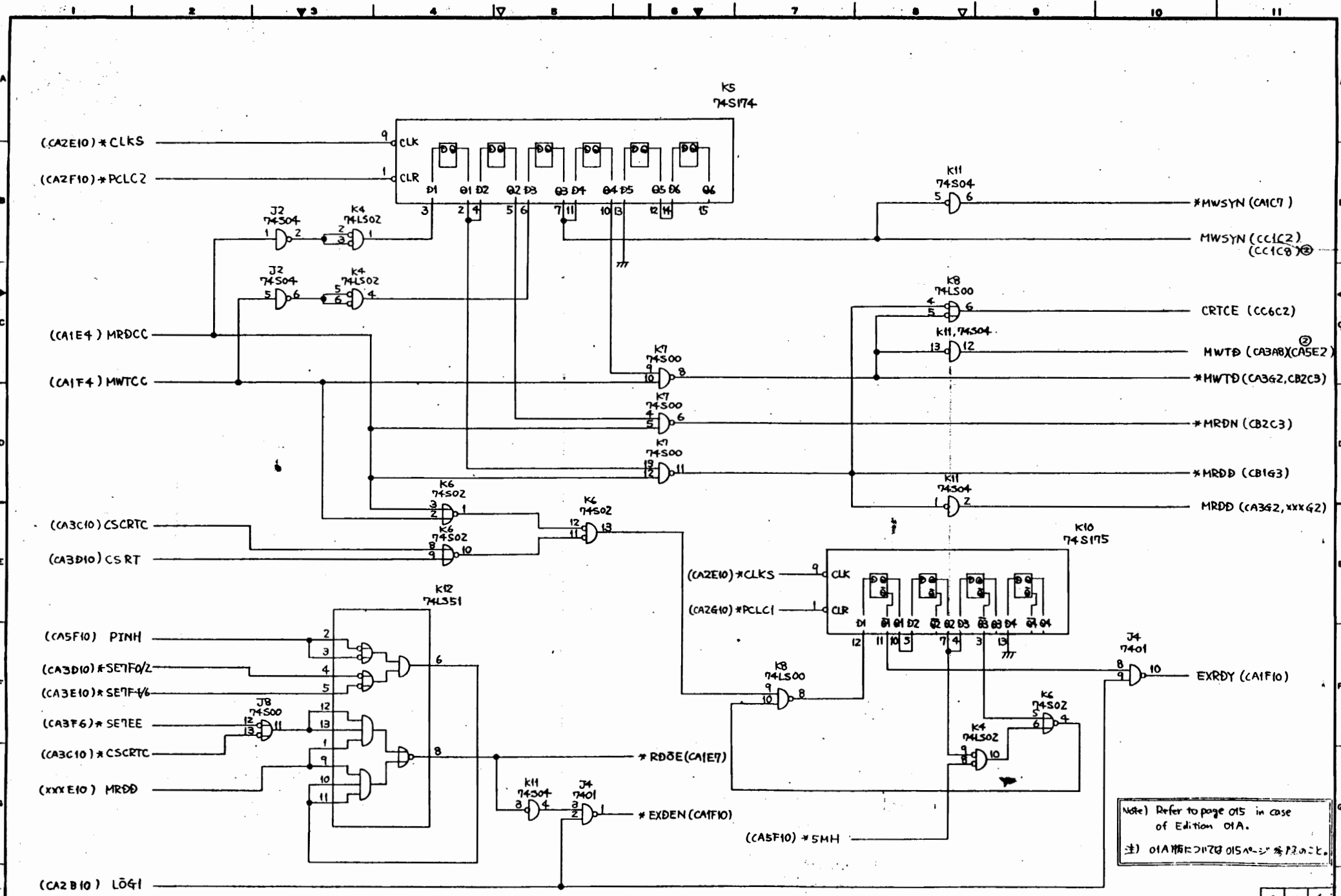
Clock. Power ON Clear



C A Z													
A20C-0008-0430/01													

REV. 31943B

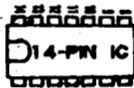
1/2
85/59



Note) Refer to page 015 in case of Edition 01A.
 注) 01A版に於いては015Aにシテ参照のこと。

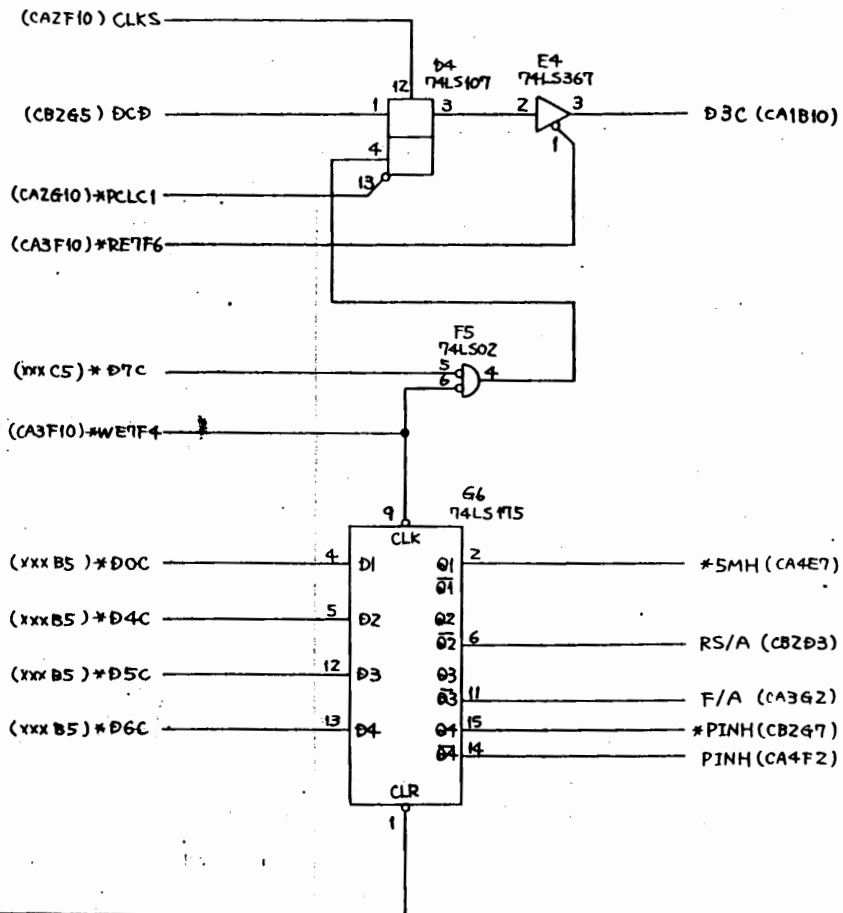
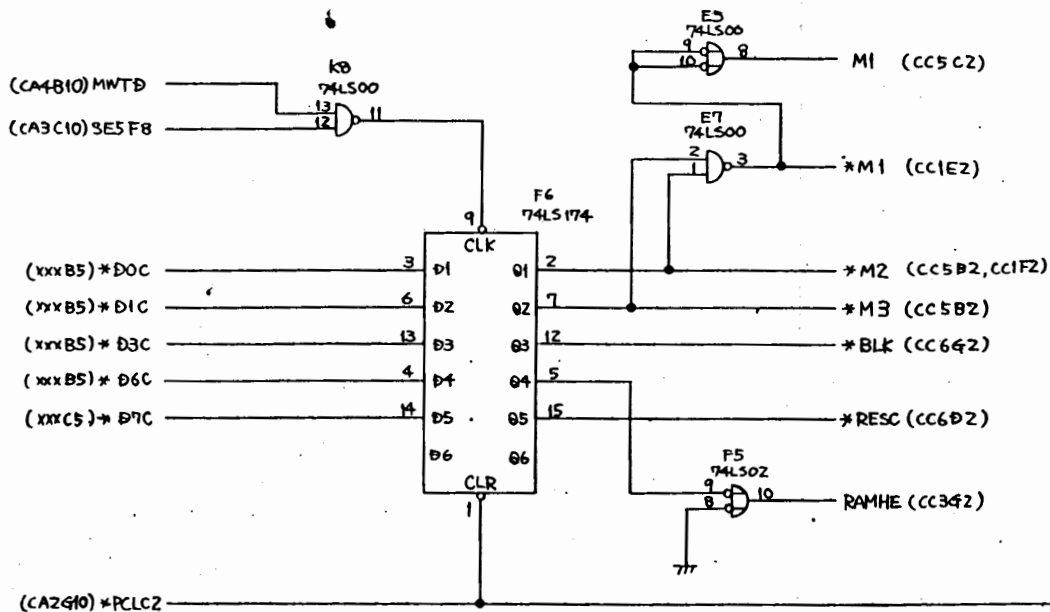
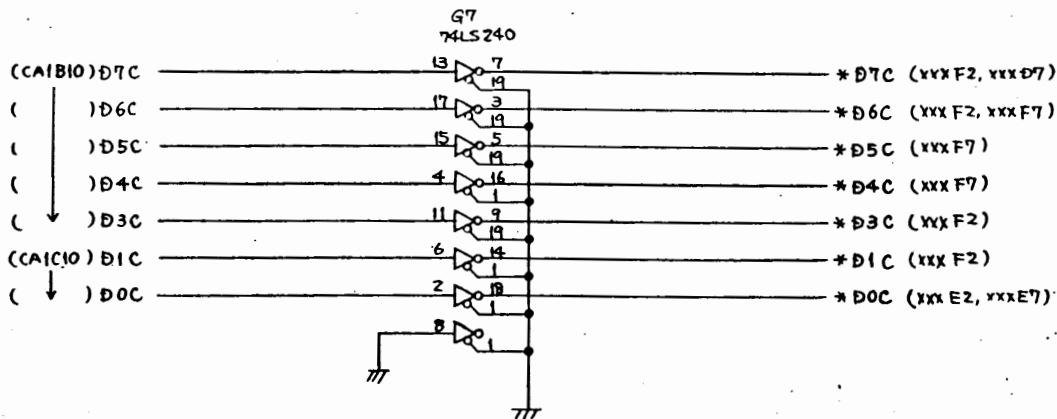
CA4

Read/Write Strobe, EXRDY for USART & CRTC

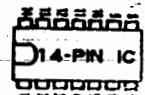


AZOC-0008-043/01

AW: 319439 90



Note) Refer to Page 016 In case of Edition 01A.
 注) 01A版に引いた016ページの図にしてください。

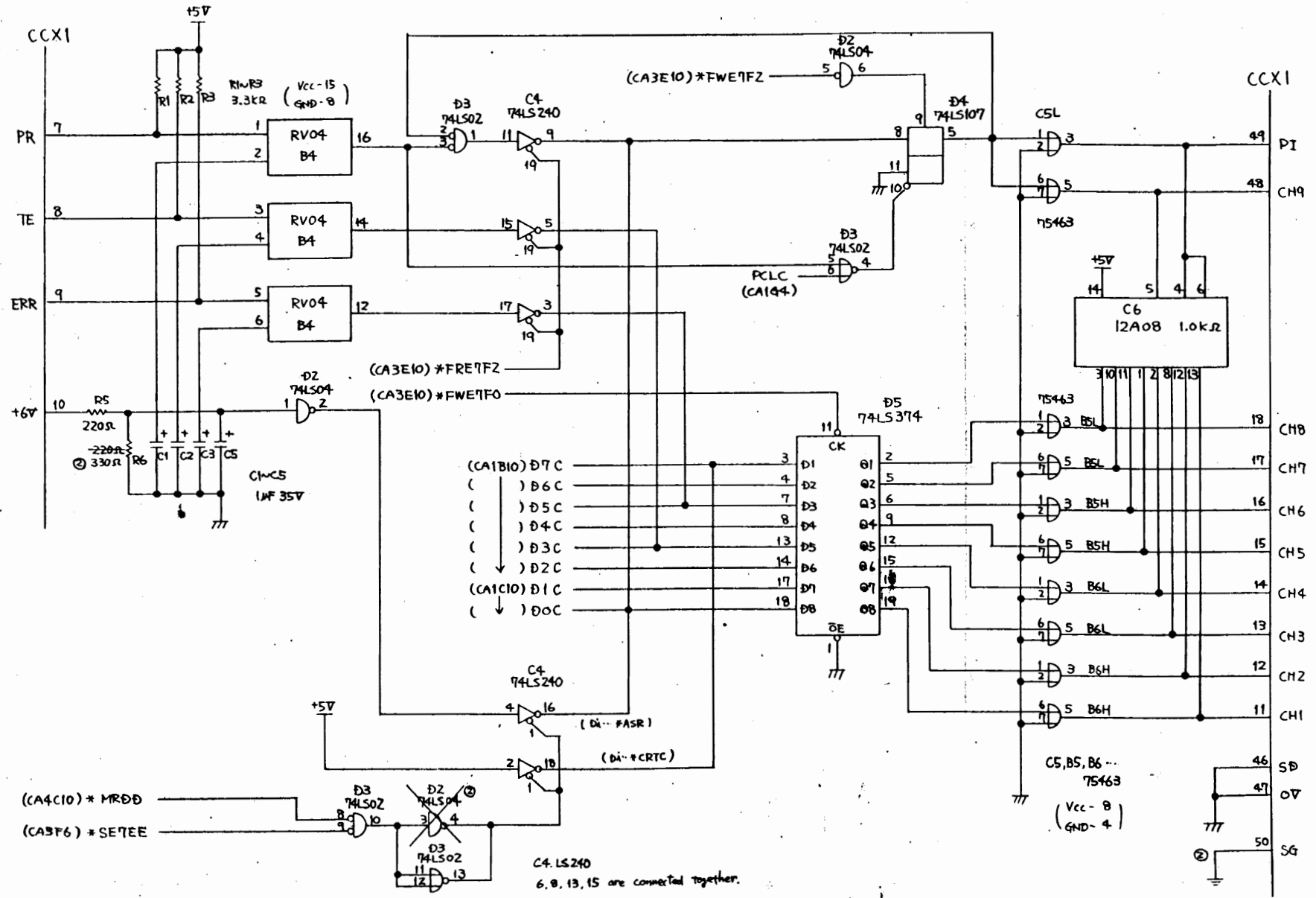


Control D0 for CRT & Puncher, D1 (*D0C)

C A 5

A20C-0008-0430/01

AWI-319440



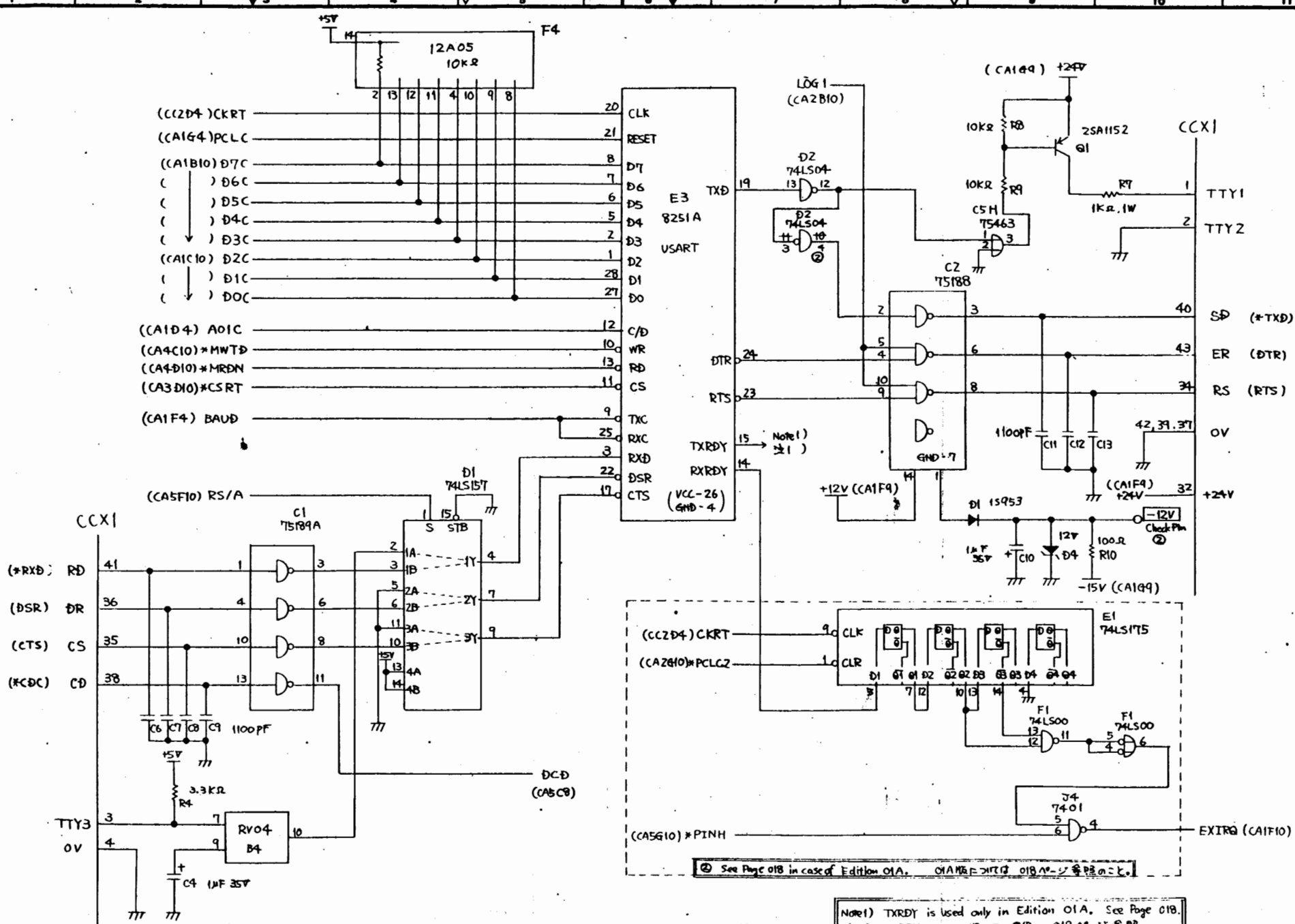
FACIT Inter face

14-PIN IC

A20C-0008-0430/01

C B 1

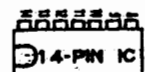
AW1-319441



② See Page 018 in case of Edition 01A. O1A版では018ページの回路のこ。

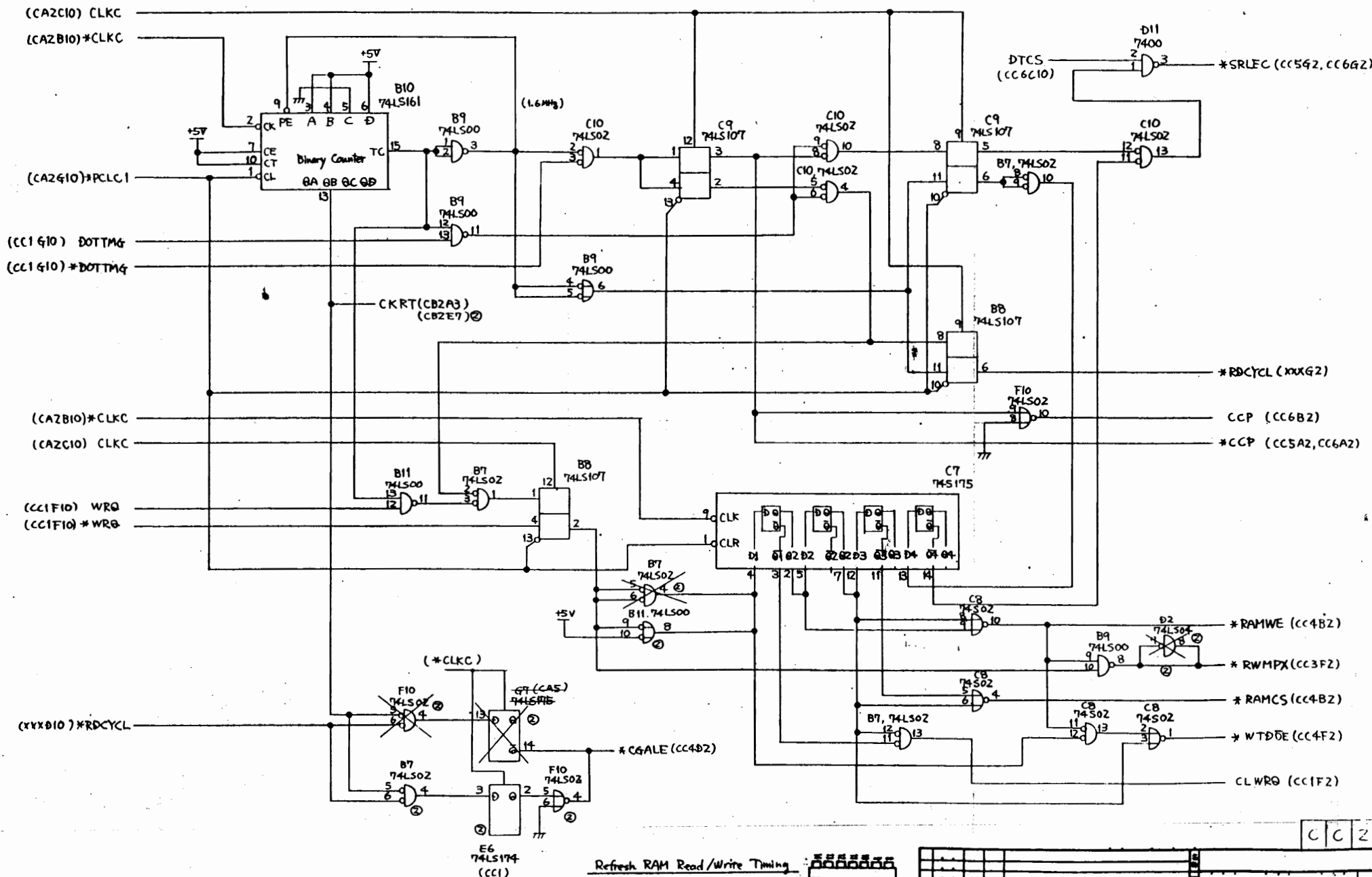
Note1) TXRDY is used only in Edition 01A. See Page 018.
 注1) TXRDYは01A版のみ使用。018ページの回路。

RS232C, ASR33 Interface



1	2	3	4	5	6	7	8	9	10	11	12	13	14
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AWI-319443 06



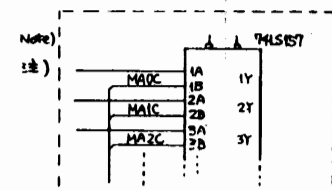
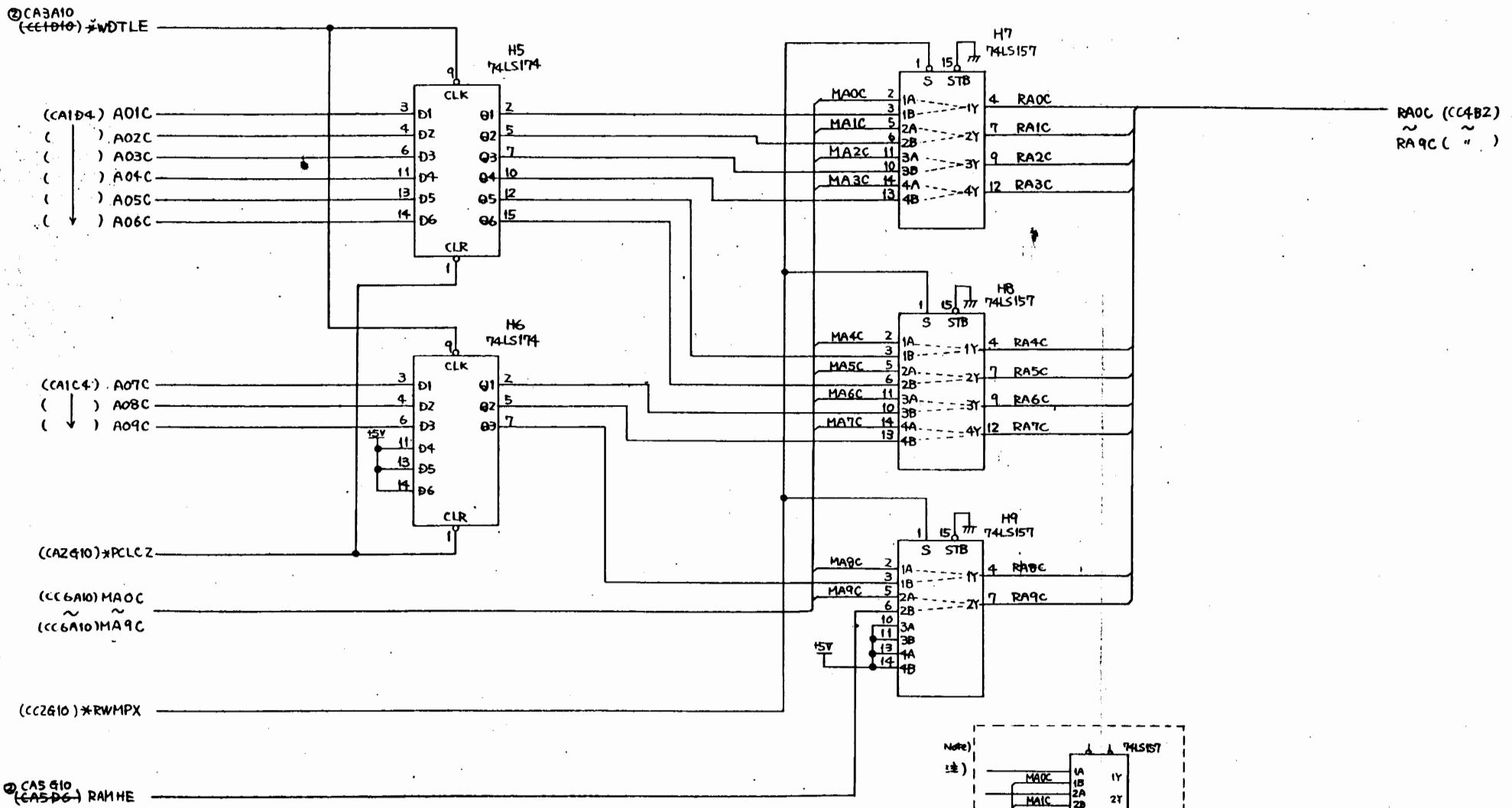
C C Z

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

13
90k

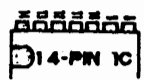
120C-0008-0430/01

AWT-319444 16



Input A and B of 74LS157's are swapped in Edition 01A.
 01A版では 74LS157の A, B の接続が逆です。

Address multiplexer for Refresh RAM's



C C 3

AW1-319446 26

(CC2E10) *CCP
(CA5F6) *M3
(CA5F6) *M2

(CC5E10) DTCTF

(CA2G10) *PCLC2

(CA5E6) M1
(CA5D5)
(CC6E10) VSYN

(CC4E10) CGA0
(CC4E10) CGA6

(CA2B10) *CLKC

(CC1G10) *DOTTM4Z

(CC2B10) *SRLE

(CA2G10) *PCLC2

+5V

E9

74LS02

E8

E10

74LS02

E10

C11

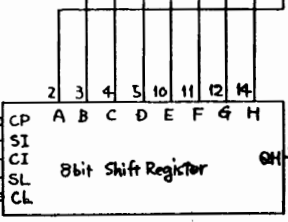
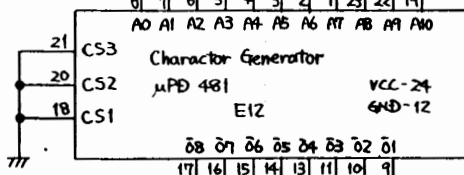
74LS00

E9

74LS02

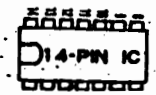
E9

74LS02

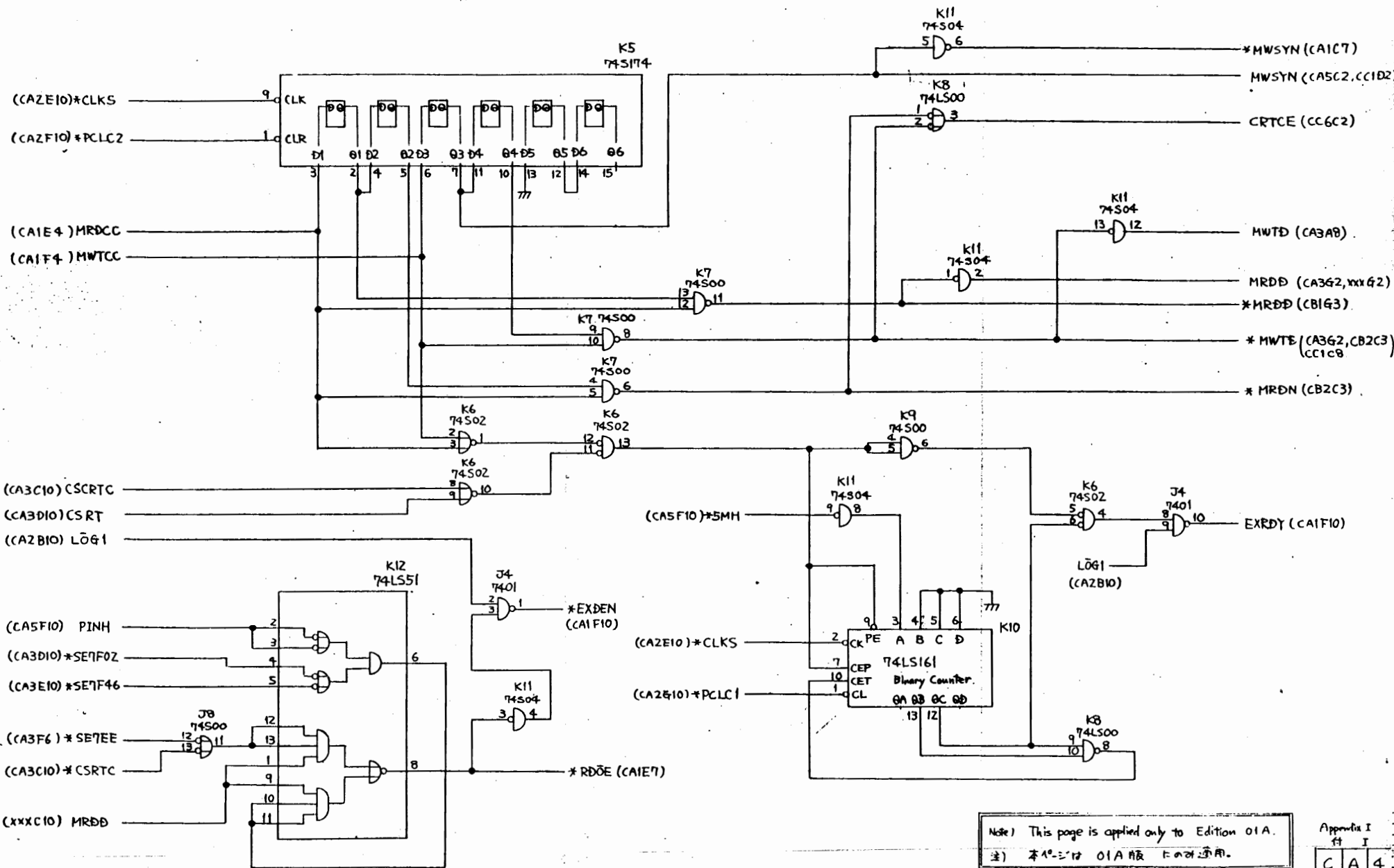


D0TFC (CC6E2)

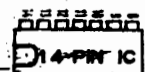
Character generator



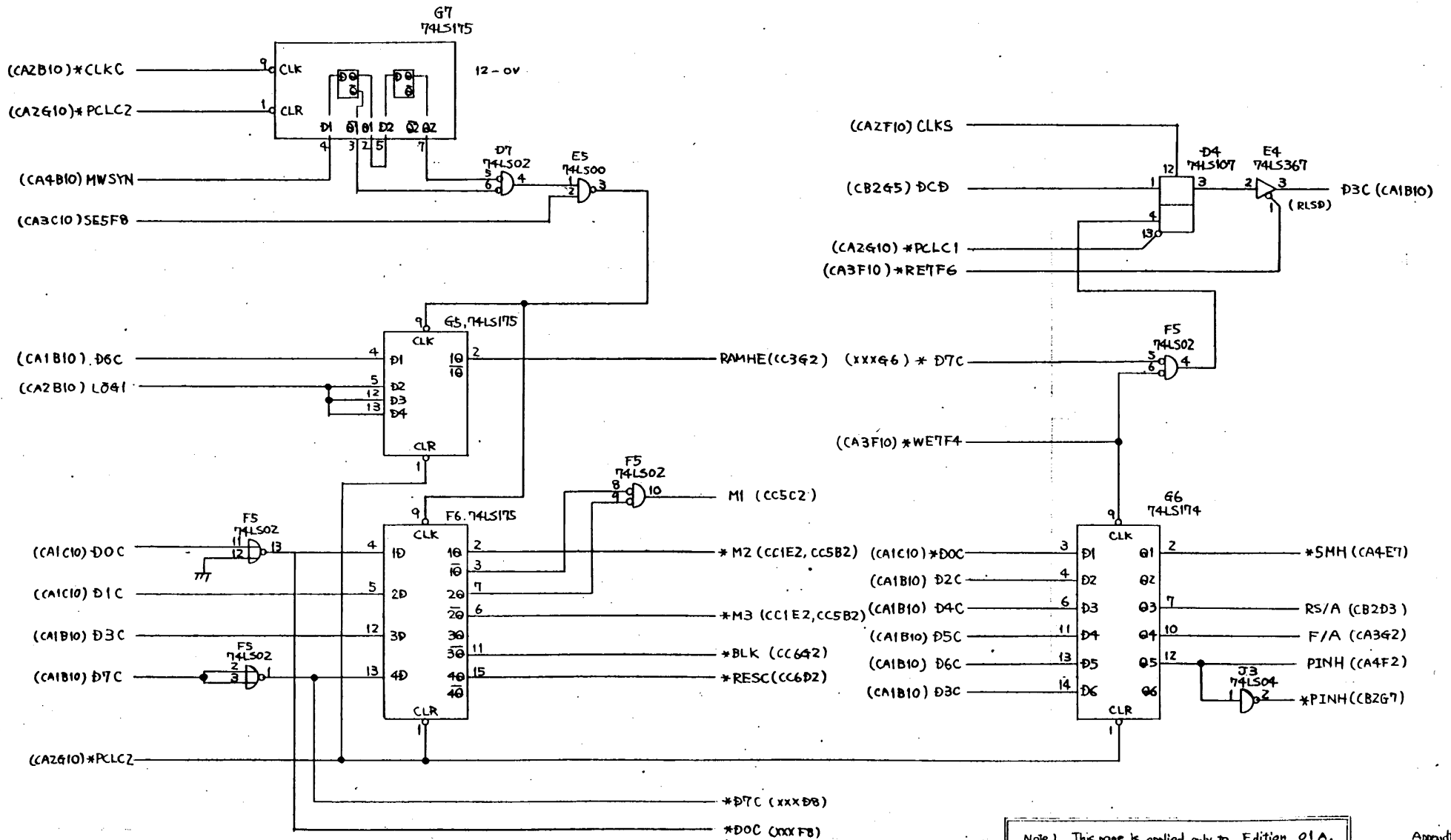
A20C-0008-0430/01



Note) This page is applied only to Edition 01A.
 注) 本ページは 01A 版 への適用。



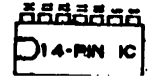
1	2	3	4	5	6	7	8	9	10	11	12	13	14

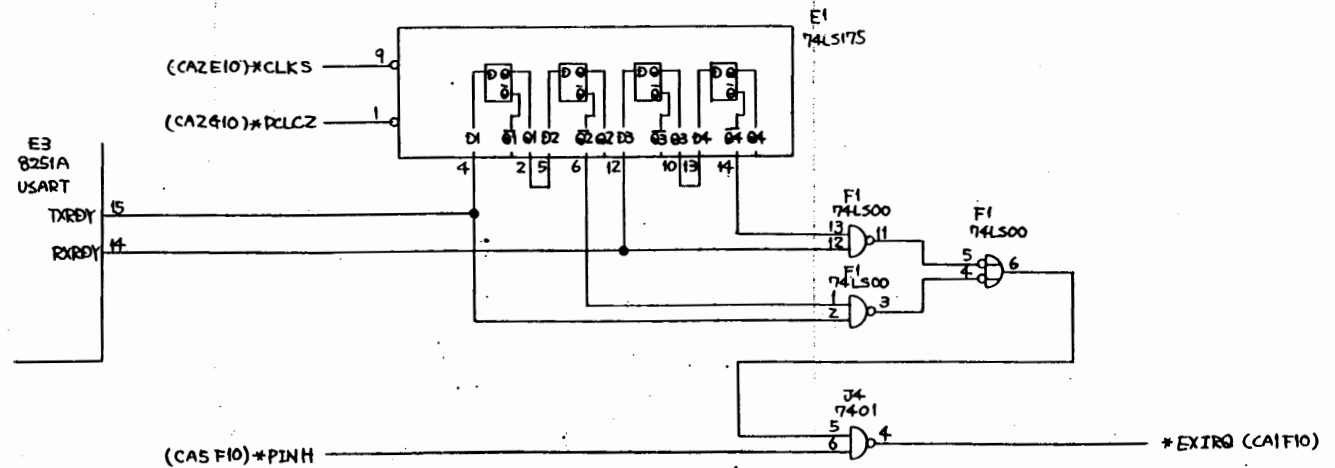


Note) This page is applied only to Edition 01A.
 注) 本ページの適用は、第01A版にのみ適用。

Appendix II
 C A 5

Control DO for CRT & Puncher, DI (RLSD)



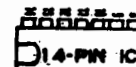


Note) This page is applied only to Edition 01A.

注) 本ページの01A版への適用のこと。

Appendix IV

C	B	Z
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1	2	3	4	5	6	7	8	9	10	11	12	13	14

A20C-0008-0430/K01